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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PTO-INBOX@AKACHANLAW.COM

Office Action Summary	Application No.	Applicant(s)	
	10/709,844	BALSDON ET AL.	
	Examiner	Art Unit	
	NAUM B. LEVIN	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-14 and 21-30* is/are pending in the application.

4a) Of the above claim(s) *9-12 and 30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7,8,13,14 and 21-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/709,844 and appeal brief filed on 02/29/2008. Claims 1-5, 7-14 and 21-30 remain pending in the application.

2. In view of the appeal brief filed on 02/29/2008, PROSECUTION IS HEREBY REOPENED (see form paragraph 12.187). New grounds of rejection are set forth below.

Election/Restrictions

3. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-5, 7-8, 13-14 and 21-29 (Group 1), drawn to routing interconnections in an integrated circuit based on electrical requirements, classified in class 716, subclass 12.

II. Claim 9-12, 30 (Group 2), drawn to designing interconnections in an integrated circuit for semiconductor mask based on optical proximity correction design rules, classified in class 716, subclass 19.

Inventions 1-5, 7-8, 13-14 and 21-29 (Group 1) and 9-12. 30 (Group 2) are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed, because Group 1 does not require using requirements of optical proximity

correction design rules. The subcombination (Group 2) has separate utilities such as: creating interconnect line having a width based on optical proximity effects.

4. Because these inventions are distinct for the reasons given above, restriction for examination purposes as indicated is proper.

5. During a telephone conversation with Attorney Melvin D. Chan (Reg. No. 39,628) on 09/09/2008 a provisional election was made of Group 1, claims 1-5, 7-8, 13-14 and 21-29 without traverse.

6. Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined (37 CFR 1.143).

7. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Objections

8. Claims 1 and 13 are objected to because following informalities:

Applicant must clarify what is “flood/flooding operation”.

9. In claim 21 Applicant must clarify what is “a first net”, “a second net”, “a third net”.

10. In claim 13 Applicant must clarify what is “determining a property of the interconnect route path”, “a design rule”.

Appropriate corrections are required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-5, 7-8 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable by Adler et al. ("A Current Driven Routing and Verification Methodology for Analog Applications", Design Automation Conference, 2000, June 5-9, 2000, page(s):385 – 389) in view of Durrill at al. (US Patent 7,168,041).

12. As to claims 1, 23 Adler discloses:

Claim 1 An electronic automation system comprising:

a database of an integrated circuit design (All data used within the integrated circuit design flow is stored in database called MGEN - page 385, right column, paragraph 5; page 388, left column, last paragraph; page 389, left column, paragraph 6; Fig.1);

a graphical user interface tool, capable of accessing and performing operations on the database, based on input (designer/user inputs/delivers manually generated stirnuli using a standard circuit simulator/graphical user interface tool for simulation of the circuit netlist. The resulting current values for all terminals are stored

into MGEN/database and used by the Current Driven Router and the Current Density Simulator, respectively/ accessing and performing operations on the database based on designer input – page 386, left column, last paragraph; page 386, right column, first paragraph; Figs.1-2); **and**

a shape-based automatic router tool (a shape-based system includes rectangle of other polygons and rectangle may be representative of any polygon of the integrated circuit, such as net, contact – Applicant's specification, paragraph 30) (using a customized algorithm (CDX) a current driven router (CDR) decomposes the wires into simple rectangles/shapes - page 388, left column, paragraphs 7-8), **capable of accessing the database** (The Current Driven Router (CDR) reads/access the netlist and the current properties from MGEN/ and performs the routes for nets – page 385, right column, paragraph 7; Fig.7), **using flood operations to create an interconnect route path for at least one net of the integrated circuit design** (As best understood, Based on the topology router/CDR calculates all unknown currents of wires connecting Steiner points/interconnect route path. Afterwards, all wires are widened/flood operation with respect to their calculated current flow … Unlike in power and ground routing CDR calculates the unknown wire widths 'on the fly'/food operation during Steiner tree based layout construction. Therefore, no post-processing steps are needed to generate design rule correct layout – page 386, right column, paragraphs 4-6; page 387, left column, paragraph 1; 'on the fly' is performed by involving obstacles/detour - page 387, right column), **selected** (Peak currents are extracted and inserted into the schematic. These currents guide the routing tool CDR in

order to generate the design rule correct layout for all multiterminal signal nets/selecting at least one net - page 385, right column, paragraph 2) **using the graphical user interface tool , wherein the interconnect route path comprises segments having different interconnect widths** (CDR tool creates non-uniform/different interconnect widths of segments – page 387, Figs.6-8);

Claim 23 An electronic design automation system comprising:

a database of an integrated circuit design (All data used within the integrated circuit design flow is stored in database called MGEN - page 385, right column, paragraph 5; page 388, left column, last paragraph; page 389, left column, paragraph 6; Fig.1);

a graphical user interface tool, capable of accessing and performing operations on the database, based on input (designer/user inputs/delivers manually generated stirnuli using a standard circuit simulator/graphical user interface tool for simulation of the circuit netlist. The resulting current values for all terminals are stored into MGEN/database and used by the Current Driven Router and the Current Density Simulator, respectively/ accessing and performing operations on the database based on designer input – page 386, left column, last paragraph; page 386, right column, first paragraph; Figs.1-2); and

a shape-based automatic router tool (a shape-based system includes rectangle of other polygons and rectangle may be representative of any polygon of the integrated circuit, such as net, contact – Applicant's specification, paragraph 30) (using a customized algorithm (CDX) a current driven router (CDR)

decomposes the wires into simple rectangles/shapes - page 388, left column, paragraphs 7-8), **capable of accessing the shape-based database** (The Current Driven Router (CDR) reads/access the netlist and the current properties from MGEN/ and performs the routes for nets – page 385, right column, paragraph 7; Fig.7), **using batched greedy algorithm to create an interconnect route path for at least one net of the integrated circuit design** (Therefore, CDR's Steiner tree algorithm has to build the Steiner tree in a greedy, sophisticated fashion/batched greedy algorithm to compute the unknown wire widths 'on the fly' during Steiner tree construction - Page 387, right column, paragraph 3) **selected** (Peak currents are extracted and inserted into the schematic. These currents guide the routing tool CDR in order to generate the design rule correct layout for all multiterminal signal nets/selecting at least one net - page 385, right column, paragraph 2) **using the graphical user interface tool, wherein the interconnect route path comprises segments having different interconnect widths** (CDR tool creates non-uniform/different interconnect widths of segments – page 387, Figs.6-8).

With respect to claims 1 and 23 Adler teaches the features above but lacks an electronic automation system comprising a mouse input device.

13. As to claims 1 and 23 Durrill recites:

An electronic automation system comprising (Abstract)**:**

a mouse input device (Abstract; col.12, ll.14-36; Fig.13).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Durrill's teaching regarding the electronic automation

system further comprising a well known in the art mouse to edit integrated circuit layout (Abstract; col.12, ll.14-36) and use it in Adler's invention, thereby achieving the same result.

14. As to claims 2, 5, 7-8 and 21-22 Adler discloses:

Claim 2 The system further comprising:

a file, accessible by the shape-based automatic route tool comprising a current density table/database including current density as a function of at least one of layer, track width (page 386, left column, paragraph 1; page 388, right column, paragraphs 1-3);

Claim 5 The system, wherein the shape-based automatic router tool uses at least one of Steiner tree algorithm, heuristic Steiner tree creation algorithm and batched greedy algorithm (page 387, left column, paragraphs 4-8; page 387, right column, paragraphs 1-3);

Claim 7 The system, wherein the integrated circuit design comprises at least analog integrated circuit (Abstract);

Claim 8 The system, wherein shape-based automatic router tool creates interconnect route paths for two or more nets located in one layer of the integrated circuit design (page 388, left column, paragraphs 4-8; page 388, right column, paragraphs 1-3; Fig.7);

Claim 21 The system, wherein automatic router tools creates interconnect route paths for a first net, a second net, and a third net carrying different signals and having different interconnect widths (page 386, right column, last paragraph;

page 387, left column, paragraphs 1-2; page 388, left column, paragraph 7; page 389, left column, paragraph 3; Fig.7).

Claim 22 The system, wherein the automatic router tool performs detailed routing (page 387, left column, paragraph 2).

15. As to claims 3 and 4 Durrill discloses:

Claims 3 The system further comprising frequency information for one or more nets of integrated circuit, wherein when frequency information is not provided for a net, DC operation of the net will be assumed (col.6; col.9, ll.35-44; col.11, ll.24-29; Figs.3, 5-6);

Claims 4 The system further comprising when frequency information is not provided for a net, a warning message is presented (col.13, ll.45-61; Figs.5-7).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 13-14 rejected under 35 U.S.C. 102(b) as being unpatentable by Adler et al. ("A Current Driven Routing and Verification Methodology for Analog Applications", Design Automation Conference, 2000, June 5-9, 2000, page(s):385 – 389).

16. As to claim 13 Adler describes:

Claim 13 A method of designing an integrated circuit comprising:

using at least one flooding operation to determine an interconnect route path between a first point and a second point of an integrated circuit design (As best understood, Based on the topology router/CDR calculates all unknown currents of wires connecting Steiner points /determine an interconnect route path between a first point and a second point. Afterwards, all wires are widened/flood operation with respect to their calculated current flow ... Unlike in power and ground routing CDR calculates the unknown wire widths 'on the fly'/food operation during Steiner tree based layout construction - page 386, right column, paragraphs 4-6; page 387, left column, paragraph 1);

determining a property of the interconnect route path (As best understood, an analog simulator is used to compute/determine the currents at all terminals - page 385, right column, paragraph 6; CDR computes the unknown current flow on connections between two Steiner points by simply adding the current flows of the two wires connection to the Steiner point. At Steiner point STI CDR has to add the current flows of terminal TI and terminal **T2** to compute the unknown current on the wire which leaves Steiner point **ST1.** At Steiner point **ST2** the current flow of terminal T3 is added to this sum and finally the current flow of terminal **T4** is added to that value at Steiner point **ST3** - page 387, right column, last paragraph; page 388, left column, paragraph 1; Fig.6)**; and**

creating an interconnect line for the interconnect route path having a width based on the property of the interconnect route path (As best understood, maximum currents per terminal are used **as** guidance/design rule for the Current Driven

Router (CDR) which is capable of routing analog multiterminal signal nets with current driven wire width based on calculated current flow – Abstract; page 387, right column, last paragraph; page 388, left column, paragraph 1; The current flow on wires are computed in order to widen all wires according to the currents imposed/design rule on them - page 387, right column, paragraph 2) **and a design rule** (We present a new methodology for current driven routing and layout verification for analog applications used to avoid defects due to electromigration/design rule - Abstract).

17. As to claim 14 Adler teaches:

Claim 14 The method, wherein the design rule addresses at least one of current density, electromigration, voltage drop (page 385, left column, paragraph 5; page 386, left column, paragraph 1).

18. Claims 24-29 are rejected under 35 U.S.C. 103(a) as being unpatentable by Adler et al. in view of Scheffer at al. (US Patent 6,543,041) and further in view of Durrill.

19. As to claims 24 and 25 Adler teaches:

Claim 24 An electronic automation system comprising:

a database of an integrated circuit design (All data used within the integrated circuit design flow is stored in database called MGEN - page 385, right column, paragraph 5; page 388, left column, last paragraph; page 389, left column, paragraph 6; Fig.1);

a graphical user interface tool, capable of accessing and performing operations on the database, based on input (designer/user inputs/delivers manually generated stirnuli using a standard circuit simulator/graphical user interface tool for

simulation of the circuit netlist. The resulting current values for all terminals are stored into MGEN/database and used by the Current Driven Router and the Current Density Simulator, respectively/ accessing and performing operations on the database based on designer input – page 386, left column, last paragraph; page 386, right column, first paragraph; Figs.1-2); and

a shape-based automatic router tool (a shape-based system includes rectangle of other polygons and rectangle may be representative of any polygon of the integrated circuit, such as net, contact – Applicant's specification, paragraph 30) (using a customized algorithm (CDX) a current driven router (CDR) decomposes the wires into simple rectangles/shapes - page 388, left column, paragraphs 7-8), **capable of accessing the database** (The Current Driven Router (CDR) reads/access the netlist and the current properties from MGEN/ and performs the routes for nets – page 385, right column, paragraph 7; Fig.7), **to create an interconnect route path for at least one net of the integrated circuit design** (path searching algorithms use CDR's database to create connection graph/interconnect route path for layout representation – page 387, left column, paragraph 3; a shortest path algorithm is employed to find a path/interconnect route path of minimum length between source and target - page 387, left column, paragraph 4; Figure 5 illustrates an example net with five terminals using only one current value per terminal for simplicity - page 387, left column, paragraphs 6-7; Figs.4-5) **selected** (Peak currents are extracted and inserted into the schematic. These currents guide the routing tool CDR in order to generate the design rule correct layout for all multiterminal signal nets/selecting at least

one net - page 385, right column, paragraph 2) **using the graphical user interface tool , wherein the interconnect route path comprises segments having different interconnect widths** (CDR tool creates non-uniform/different interconnect widths of segments – page 387, Figs.6-8);

Claim 25 An electronic automation system comprising:

a database of an integrated circuit design (All data used within the integrated circuit design flow is stored in database called MGEN - page 385, right column, paragraph 5; page 388, left column, last paragraph; page 389, left column, paragraph 6; Fig.1);

a graphical user interface tool, capable of accessing and performing operations on the database, based on input (designer/user inputs/delivers manually generated stirnuli using a standard circuit simulator/graphical user interface tool for simulation of the circuit netlist. The resulting current values for all terminals are stored into MGEN/database and used by the Current Driven Router and the Current Density Simulator, respectively/ accessing and performing operations on the database based on designer input – page 386, left column, last paragraph; page 386, right column, first paragraph; Figs.1-2); **and**

a shape-based automatic router tool (a shape-based system includes rectangle of other polygons and rectangle may be representative of any polygon of the integrated circuit, such as net, contact – Applicant's specification, paragraph 30) (using a customized algorithm (CDX) a current driven router (CDR) decomposes the wires into simple rectangles/shapes - page 388, left column,

paragraphs 7-8), **capable of accessing the database** (The Current Driven Router (CDR) reads/access the netlist and the current properties from MGEN/ and performs the routes for nets – page 385, right column, paragraph 7; Fig.7), **to create an interconnect route path for at least one net of the integrated circuit design** (path searching algorithms use CDR's database to create connection graph/interconnect route path for layout representation – page 387, left column, paragraph 3; a shortest path algorithm is employed to find a path/interconnect route path of minimum length between source and target - page 387, left column, paragraph 4; Figure 5 illustrates an example net with five terminals using only one current value per terminal for simplicity - page 387, left column, paragraphs 6-7; Figs.4-5) **selected** (Peak currents are extracted and inserted into the schematic. These currents guide the routing tool CDR in order to generate the design rule correct layout for all multiterminal signal nets/selecting at least one net - page 385, right column, paragraph 2) **using the graphical user interface tool , wherein the interconnect route path comprises segments having different interconnect widths** (CDR tool creates non-uniform/different interconnect widths of segments – page 387, Figs.6-8).

With respect to claims 24 and 25 Adler teaches the features above but lacks an electronic automation system further comprising file that includes frequency information for nets of the integrated circuit.

20. As to claims 24 and 25 Scheffer recites:

Claim 24 An electronic automation system comprising (Fig.6)**:**

a mouse input device (col.6, ll.41-45; Fig.6);

a file, accessible by the automatic router tool (for a given local net, in step 404 automatic router tool/process uses/access provided data/file – col.4, ll.47-62**),** **comprising a current density table comprising current density as a function of net frequency** (current density limits on the routing layers in the netlist/table are indexed/function by frequency. The current density on vias, which is used to connect between the routing layers, are also indexed/function by frequency - col.4, ll.63-67; col.5, ll.1-9);

Claim 25 An electronic automation system comprising (Fig.6)**:**

a mouse input device (col.6, ll.41-45; Fig.6);

a file, accessible by the automatic router tool (for a given local net, in step 404 automatic router tool/process uses/access provided data/file – col.4, ll.47-62)**,,** **comprising frequency information for one or more nets of integrated circuit** (current density limits on the routing layers in the netlist/table are indexed by frequency/frequency information. The current density on vias, which is used to connect between the routing layers, are also indexed by frequency/frequency information - col.4, ll.63-67; col.5, ll.1-9).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Scheffer I's teaching regarding the electronic automation system further comprising file that includes frequency information for nets of the integrated circuit and use it in Adler's invention to form a physical layout for a circuit design with improved signal integrity and reliability in the post-routing stage (col.1, ll.63-67).

21. As to claims 28 and 29 Adler discloses:

Claims 28-29 The system, wherein the shape-based automatic router tool uses a batched greedy algorithm (page 387, left column, paragraphs 4-8; page 387, right column, paragraphs 1-3),

22. As to claims 26-27 Durrill discloses:

Claim 26 The system further comprising frequency information for one or more nets of integrated circuit, wherein when frequency information is not provided for a net, DC operation of the net will be assumed (col.6; col.9, ll.35-44; col.11, ll.24-29; Figs.3, 5-6);

Claim 27 The system further comprising when frequency information is not provided for a net, a warning message is presented (col.13, ll.45-61; Figs.5-7).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NAUM B. LEVIN whose telephone number is (571)272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jack Chiang/
Supervisory Patent Examiner, Art Unit 2825

/Naum Levin/
Examiner
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